

As an inventor named below or on an attached continuation page, I hereby declare that:

My residence, post office address and citizenship are as stated next to my name.

I believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled **METHOD FOR IN-LINE TESTING OF FLIP-CHIP SEMICONDUCTOR ASSEMBLIES**, the specification of which (check one):

☒ is attached hereto.

☐ was filed on _____ as United States application serial no. _____ and was amended on _____.

☐ was filed on _____ as PCT international application no. _____ and was amended under PCT Article 19 on _____.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to the patentability of the subject matter claimed in this application, as "materiality" is defined in Title 37, Code of Federal Regulations § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate or § 365(a) of any PCT international application(s) designating at least one country other than the United States of America listed below and on any attached continuation page and have also identified below and on any attached continuation page any foreign application for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America having a filing date before that of the application(s) on which priority is claimed:

Prior foreign/PCT application(s):

(number)	(country)	(day/month/year filed)	Priority Claimed	
			Yes	No
_____	_____	_____	_____	_____
_____	_____	_____	_____	_____

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) or § 365(c) of PCT international application(s) designating the United States of America listed below and on any attached continuation page and, insofar as the subject matter of each of the claims of this application is not disclosed in any such prior application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations § 1.56 which became available between the filing date of such prior application and the national or PCT international filing date of this application:

(application serial no.)	(filing date)	(status - pending, patented or abandoned)
_____	_____	_____
_____	_____	_____

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below:

(provisional application no.)	(filing date)
_____	_____
_____	_____
_____	_____

I hereby appoint the following Registered Practitioners to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Date

9/28/98

Invention title: METHOD FOR IN-PROCESS TESTING OF FLIP-CHIP SEMICONDUCTOR ASSEMBLIES

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Cobbley et al.

Serial No.: To be assigned

Filed: October 29, 2002

For: METHOD FOR MANUFACTURING
FLIP-CHIP SEMICONDUCTOR ASSEMBLY

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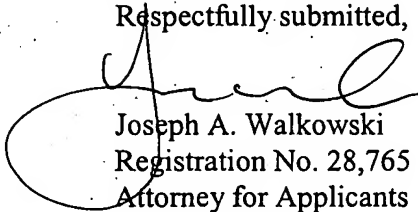
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Commissioner for Patents
Washington, D.C. 20231

Sir:

In accordance with 37 C.F.R. § 1.34(b), please recognize the following individual as an associate agent/attorney herein in connection with the above-identified patent application, and with all continuing and divisional applications hereof:

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Respectfully submitted,


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